## CLAIMS

## What is claimed is:

- 1 1. A semiconductor device comprising:
- 2 an active region of a first conducting type including a transistor structure,
- 3 a ring shaped region of the first conducting type extending from a surface of the active
- 4 region into the active region and substantially surrounding the transistor structure.
- 1 2. The device as in claim 1, wherein the transistor structure comprises, a drain region, a
- 2 source region, wherein the drain and the source define a channel, a gate being arranged
- 3 above said channel, and a sinker structure of said first conducting type arranged
- 4 substantially along said source region reaching from the surface of the active area next to the
- 5 source region to the bottom of the active area.
- 1 3. The device as in claim 2, wherein the p ring is less doped than the sinker structure.
- 1 4. The device as in claim 2, wherein the drain region comprises a lightly doped drain
- 2 region.
- 1 5. The device as in claim 4, further comprising a metal layer on the backside of the
- 2 semiconductor device.
- 1 6. The device as in claim 1, wherein the transistor structure is a two transistor structure
- 2 comprising, a common drain region, a first source region arranged on one side of the
- 3 common drain region, a second source region arranged on the respective opposite side of the
- 4 drain region, wherein the drain region and the source regions each define a channel, a first
- 5 and second gate being arranged above said channels, and a first and second sinker structure
- 6 of said first conducting type arranged substantially along said source regions reaching from
- 7 the surface of the active area next to the respective source regions to the bottom of the active
- 8 area.
- 1 7. The device as in claim 5, wherein the drain region comprises a lightly doped drain
- 2 region.

- 1 8. The device as in claim 5, further comprising a metal layer on the backside of the
- 2 semiconductor device.
- 1 9. The device as in claim 5, wherein the ring is less doped than the sinker structure.
- 1 10. The device as in claim 1, wherein the ring is doped in the range of  $10^{14}$ - $10^{15}$ /cm<sup>2</sup>.
- 1 11. The device as in claim 1, wherein the active area is created and enclosed by a
- 2 LOCOS process.
- 1 12. The device as in claim 11, wherein the active area comprises a substrate and an
- 2 epitaxial layer on top of said substrate.
- 1 13. The device as in claim 1, wherein the first conducting type is the p type.
- 1 14. The device as in claim 1, wherein the ring is created by masked ion implant.
- 1 15. The device as in claim 10 wherein boron is used as a dopant.
- 1 16. The device as in claim 1, wherein the ring has a rectangular, circular, oval, or
- 2 polygon shape.
- 1 17. The device as in claim 1, wherein the ring comprises at least one gap that does not
- 2 substantially influence an insulating function of the ring.

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- 1 18. A semiconductor device comprising:
- 2 an active region of a first conducting type including a transistor structure, wherein the
- 3 transistor structure comprises, a drain region of a second type, a channel, and a gate being
- 4 arranged above said channel, and
- 5 a ring shaped region of the first conducting type extending from a surface of the active
- 6 region into the active region and surrounding the transistor structure.
- 1 19. The device as in claim 18, further comprising a source region of the second type
- 2 arranged along one side of the drain region, and a sinker structure of said first conducting
- 3 type arranged substantially along said source region reaching from the surface of the active
- 4 area next to the source region to the bottom of the active area.
- 1 20 The device as in claim 19, further comprising a second source region arranged on
- 2 the respective opposite side of the drain region, wherein the drain region and the source
- 3 regions each define a channel, a first and second gate being arranged above said channels,
- 4 and a first and second sinker structure of said first conducting type arranged substantially
- 5 along said source regions reaching from the surface of the active area next to the respective
- 6 source regions to the bottom of the active area.
- 1 21. The device as in claim 18, wherein the drain region comprises a lightly doped drain
- 2 region.
- 1 22. The device as in claim 19, further comprising a metal layer on the backside of the
- 2 semiconductor device.
- 1 23. The device as in claim 19, wherein the ring is less doped than the sinker structure.
- 1 24. The device as in claim 18, wherein the ring is doped in the range of  $10^{14}$ - $10^{15}$ /cm<sup>2</sup>.
- 1 25. The device as in claim 18, wherein the active area is created and enclosed by a
- 2 LOCOS process.
- 1 26. The device as in claim 25, wherein the active area comprises a substrate and an
- 2 epitaxial layer on top of said substrate.

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- **PATENT**
- The device as in claim 18, wherein the first conducting type is the p type. 1 27.
- The device as in claim 18, wherein the ring is created by masked ion implant. 1 28.
- The device as in claim 24, wherein boron is used as a dopant. 1 29.
- The device as in claim 18, wherein the ring has a rectangular, circular, oval, 1 30.
- 2 polygon, or partially open shape.
- 1 31. The device as in claim 18, wherein the ring comprises at least one gap that does not
- 2 substantially influence an insulating function of the ring.

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- 1 32. A method of manufacturing a semiconductor device comprising the steps of:
- 2 forming an active region of a first conducting type within a semiconductor material;
- 3 forming a transistor structure, and
- 4 forming a ring shaped region of the first conducting type extending from a surface of the
- 5 active region into the active region and surrounding the transistor structure.
- 1 33. The method as in claim 32, wherein the step of forming a transistor structure
- 2 comprises the steps of forming a drain region of a second type, a source region of the second
- 3 type arranged along one side of the drain region, and a sinker structure of said first
- 4 conducting type arranged substantially along said source region reaching from the surface of
- 5 the active area next to the source region to the bottom of the active area.
- 1 34. The method as in claim 33, further comprising the step of forming a second source
- 2 region arranged on the respective opposite side of the drain region, and a first and second
- 3 sinker structure of said first conducting type arranged substantially along said source regions
- 4 reaching from the surface of the active area next to the respective source regions to the
- 5 bottom of the active area.
- 1 35. The method as in claim 32, wherein the drain region is formed in such a way that it
- 2 comprises a lightly doped drain region.
- 1 36. The method as in claim 33, further comprising the step of arranging a metal layer on
- 2 the backside of the semiconductor device.
- 1 37. The device as in claim 32, wherein the step of forming the ring includes the step of
- 2 doping the ring less than the sinker structure.
- 1 38. The method as in claim 32, wherein the ring is doped in the range of  $10^{14}$ - $10^{15}$ /cm<sup>2</sup>.
- 1 39. The method as in claim 32, wherein the active area is created and enclosed by a
- 2 LOCOS process.
- 1 40. The method as in claim 32, wherein the ring is created by masked ion implant.

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- 1 41. The method as in claim 32, wherein boron is used as a dopant.
  - 42. The method as in claim 32, wherein the ring has a rectangular, circular, oval, polygon, or partially open shape.